



ALPHA & OMEGA
SEMICONDUCTOR

AONS66923

100V N-Channel AlphaSGT™

General Description

- Trench Power AlphaSGT™ technology
- Low $R_{DS(ON)}$
- Logic Level Driving
- Excellent $Q_G \times R_{DS(ON)}$ Product (FOM)
- Spike Optimized Process
- RoHS and Halogen-Free Compliant

Applications

- High Frequency Switching and Synchronous Rectification

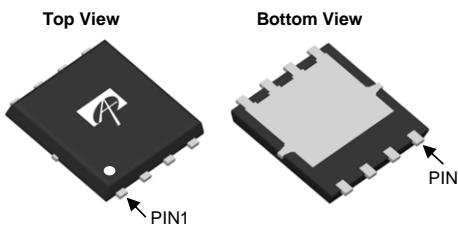
Product Summary

V_{DS}	100V
I_D (at $V_{GS}=10V$)	47A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 10.8mΩ
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 14.8mΩ

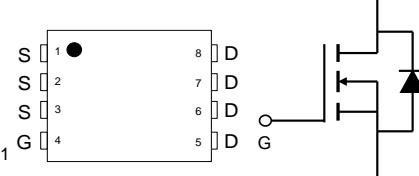
100% UIS Tested
100% R_g Tested



DFN5X6



Top View



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONS66923	DFN 5x6	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^A	I_D	47	A
$T_C=100^\circ\text{C}$		30	
Pulsed Drain Current ^C	I_{DM}	105	
Continuous Drain Current ^A	I_{DSM}	15	A
$T_A=70^\circ\text{C}$		12	
Avalanche Current ^C	I_{AS}	30	A
Avalanche energy ^C	E_{AS}	45	mJ
Power Dissipation ^B	P_D	48	W
$T_C=100^\circ\text{C}$		19	
Power Dissipation ^A	P_{DSM}	5.0	W
$T_A=70^\circ\text{C}$		3.2	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A $t \leq 10s$	$R_{\theta JA}$	20	25	°C/W
Maximum Junction-to-Ambient ^{A,D} Steady-State		45	55	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	2.1	2.6	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	100			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$		1	5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.6	2.1	2.6	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=20\text{A}$ $T_J=125^\circ\text{C}$	9.0	15.8	19.3	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=20\text{A}$		11.5	14.8	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		50		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.72	1	V
I_S	Maximum Body-Diode Continuous Current				47	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=50\text{V}, f=1\text{MHz}$		1725		pF
C_{oss}	Output Capacitance			360		pF
C_{rss}	Reverse Transfer Capacitance			7.5		pF
R_g	Gate resistance	$f=1\text{MHz}$	0.3	0.8	1.3	Ω
SWITCHING PARAMETERS						
$Q_{g(10\text{V})}$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=50\text{V}, I_D=20\text{A}$		25	35	nC
$Q_{g(4.5\text{V})}$	Total Gate Charge			12.5	18	nC
Q_{gs}	Gate Source Charge			6		nC
Q_{gd}	Gate Drain Charge			3.5		nC
Q_{oss}	Output Charge	$V_{GS}=0\text{V}, V_{DS}=50\text{V}$		30		nC
$t_{D(\text{on})}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=50\text{V}, R_L=2.5\Omega, R_{\text{GEN}}=3\Omega$		8.5		ns
t_r	Turn-On Rise Time			3		ns
$t_{D(\text{off})}$	Turn-Off Delay Time			23		ns
t_f	Turn-Off Fall Time			3.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}, di/dt=500\text{A}/\mu\text{s}$		41		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, di/dt=500\text{A}/\mu\text{s}$		156		nC

A. The value of R_{JJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{ C}$. The Power dissipation P_{DSM} is based on $R_{\text{JJA}} \leq 10\text{s}$ and the maximum allowed junction temperature of 150° C . The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{ C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{ C}$.

D. The R_{JJA} is the sum of the thermal impedance from junction to case R_{JJC} and case to ambient.

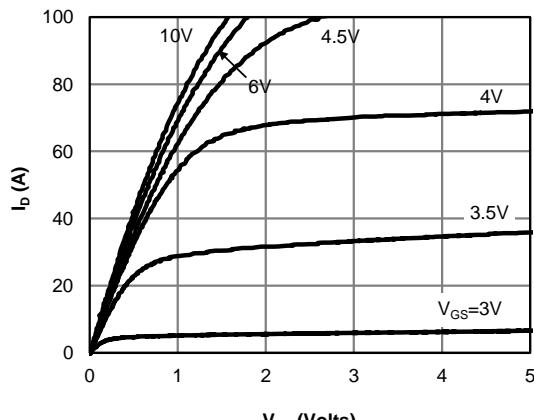
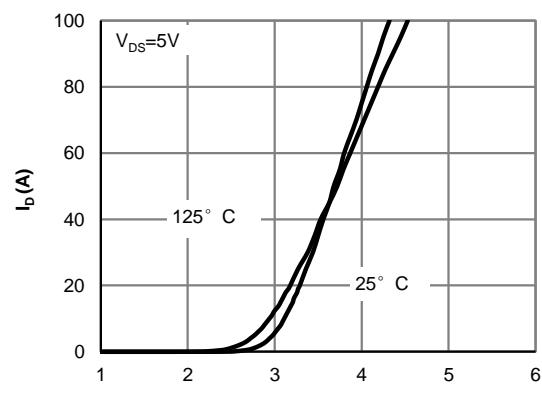
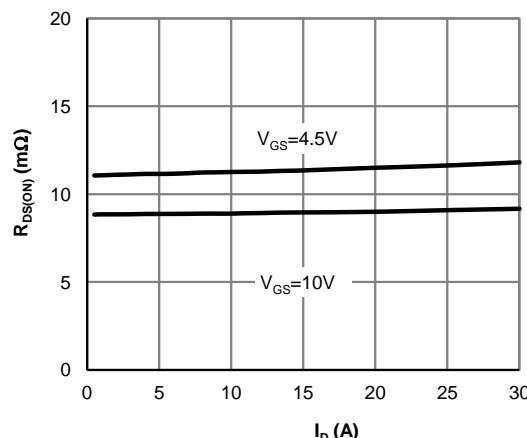
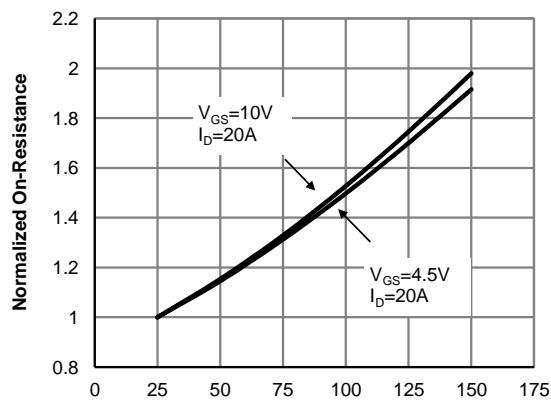
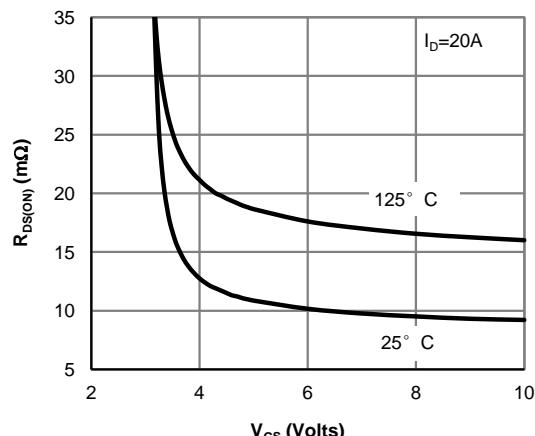
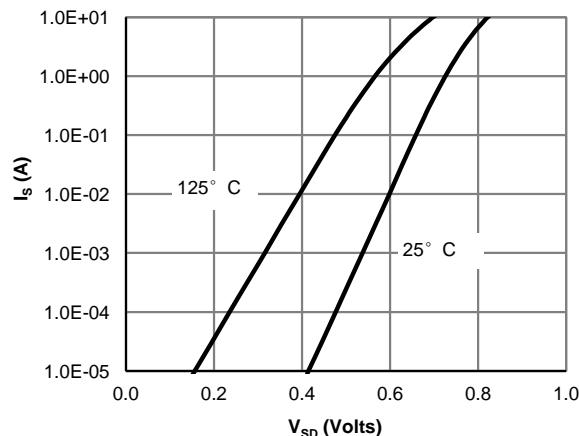
E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

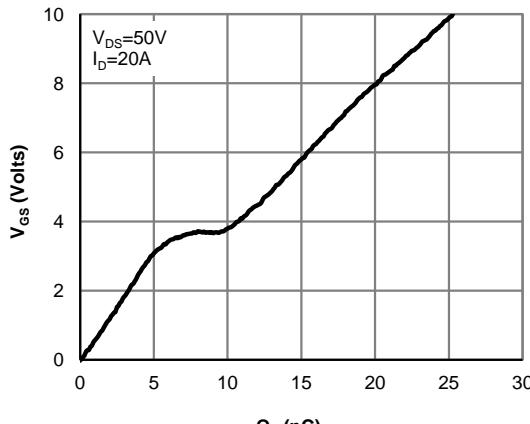
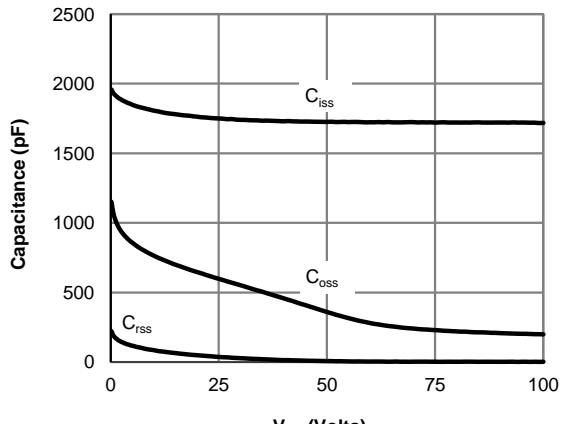
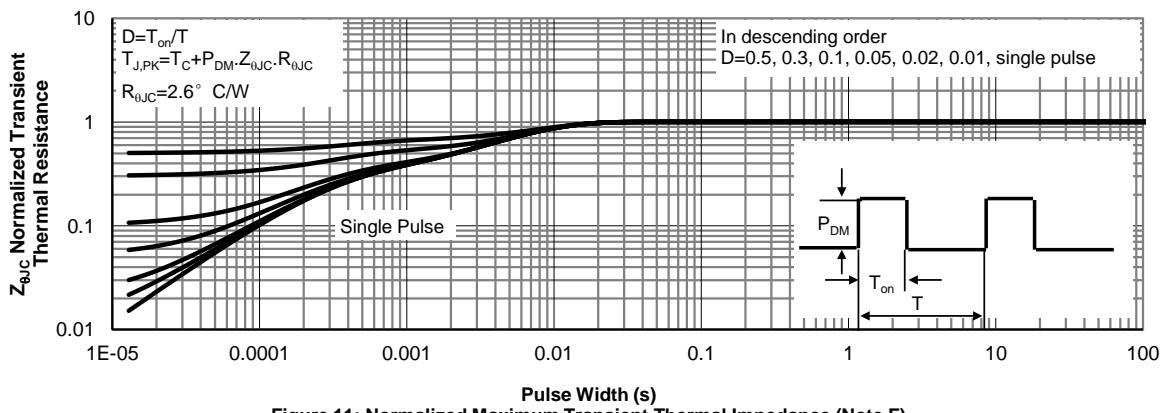
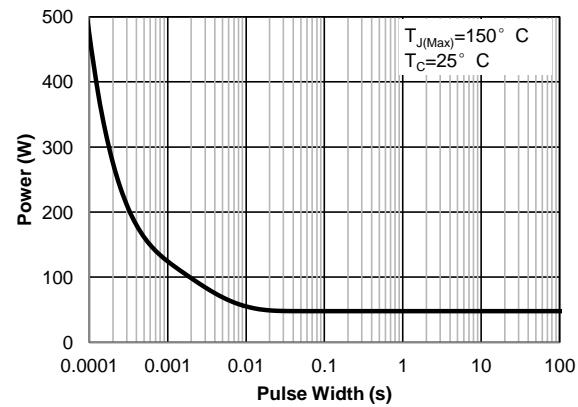
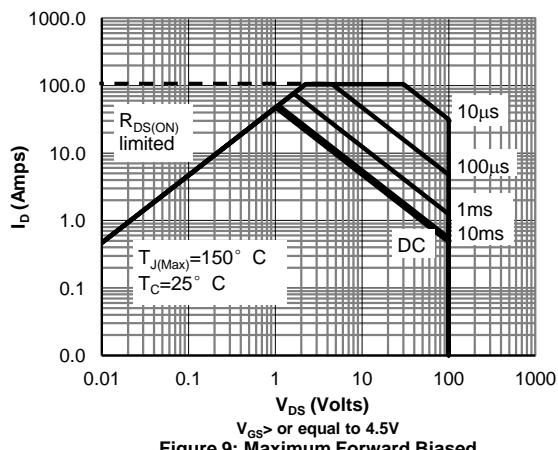
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=150^\circ\text{ C}$. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{ C}$.

APPLICATIONS OR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics


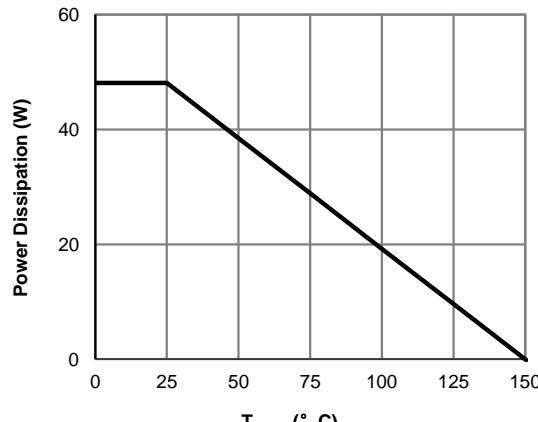
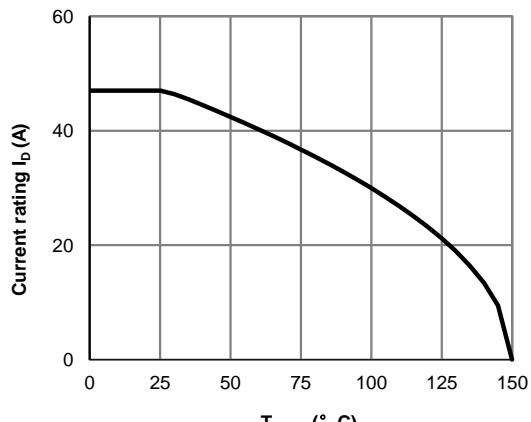
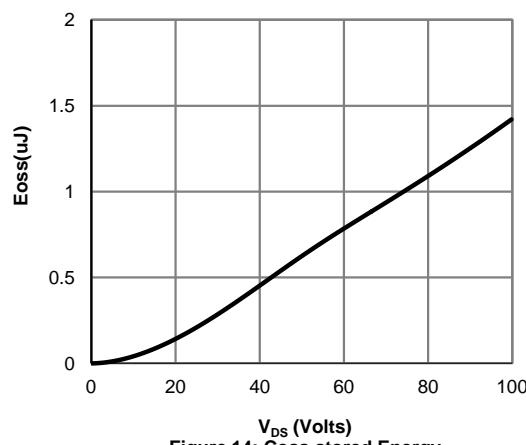
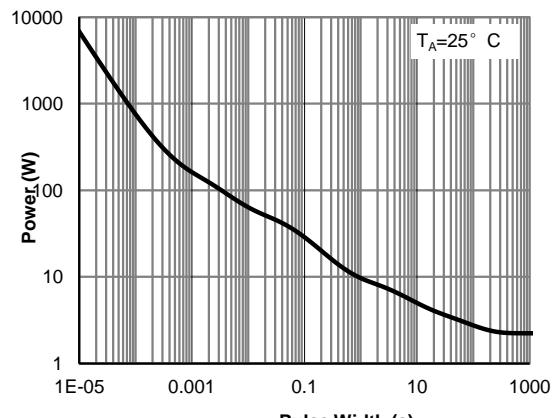
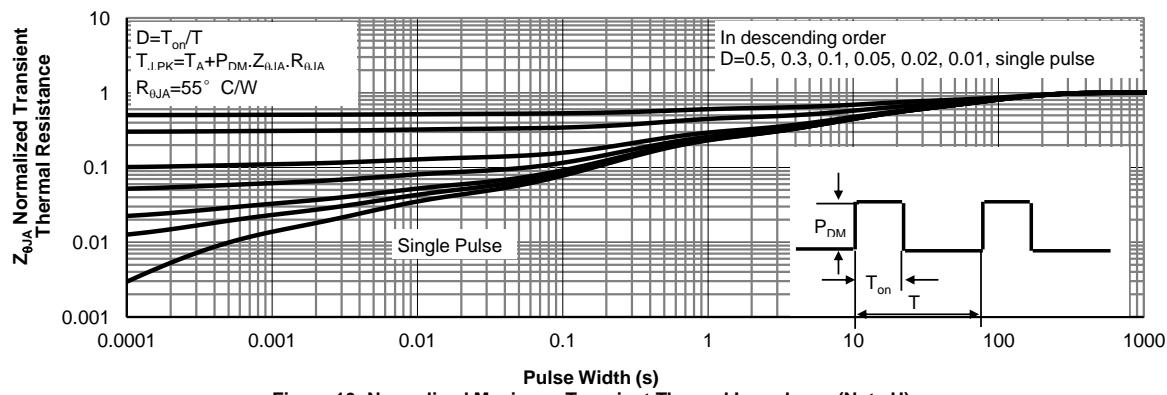
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 12: Power De-rating (Note F)

Figure 13: Current De-rating (Note F)

Figure 14: Coss stored Energy

Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

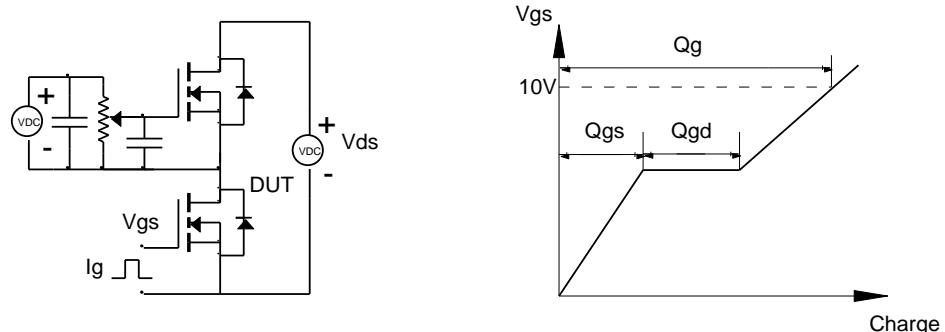


Figure B: Resistive Switching Test Circuit & Waveforms

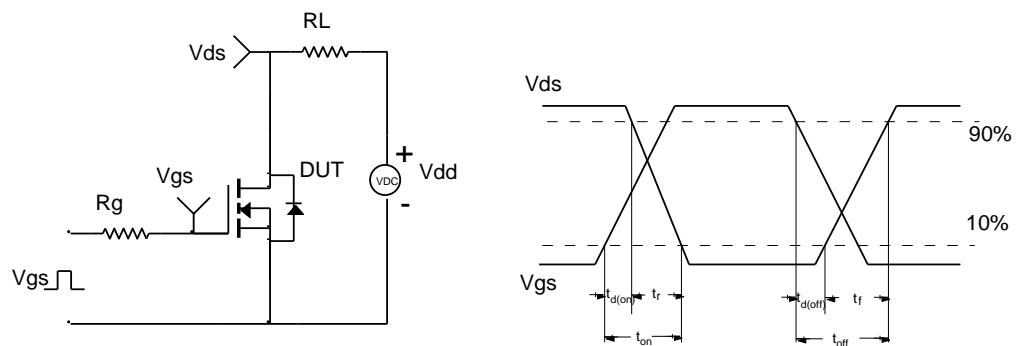


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

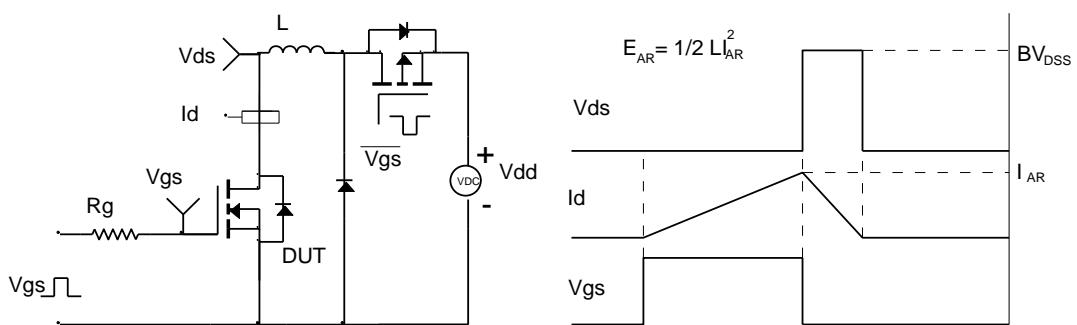
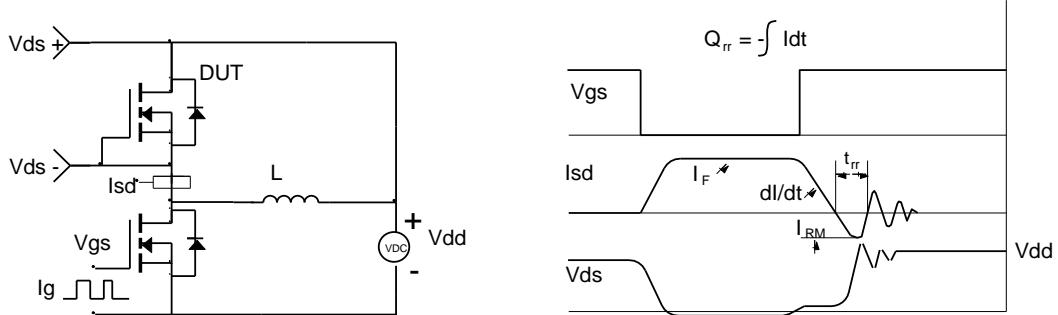


Figure D: Diode Recovery Test Circuit & Waveforms

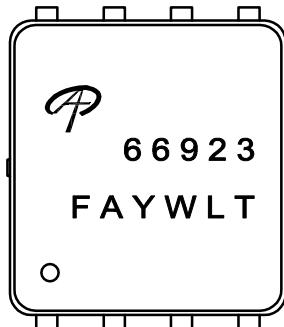




ALPHA & OMEGA
SEMICONDUCTOR

Document No.	PD-02930
Version	A
Title	AONS66923 Marking Description

DFN5x6 PACKAGE MARKING DESCRIPTION



Green product

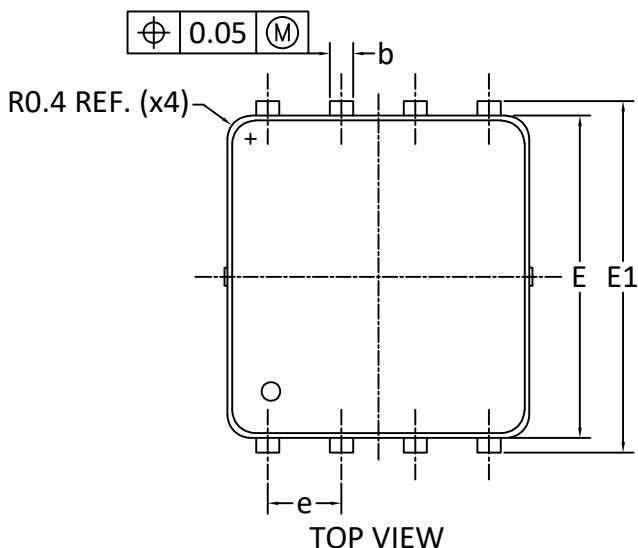
NOTE:

LOGO	- AOS Logo
66923	- Part number code
F	- Fab code
A	- Assembly location code
Y	- Year code
W	- Week code
L&T	- Assembly lot code

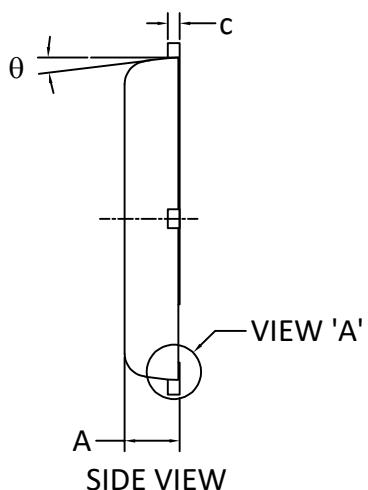
PART NO.	DESCRIPTION	CODE
AONS66923	Green product	66923



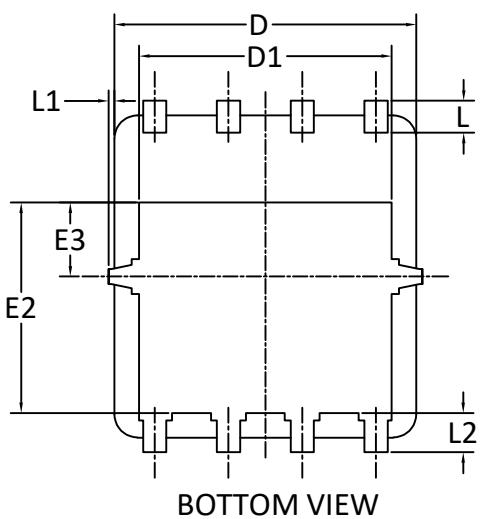
DFN5x6_8L_EP1_P PACKAGE OUTLINE



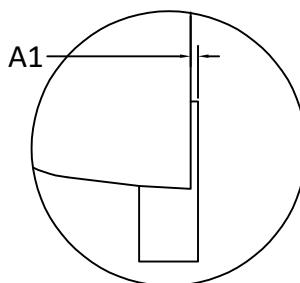
TOP VIEW



SIDE VIEW

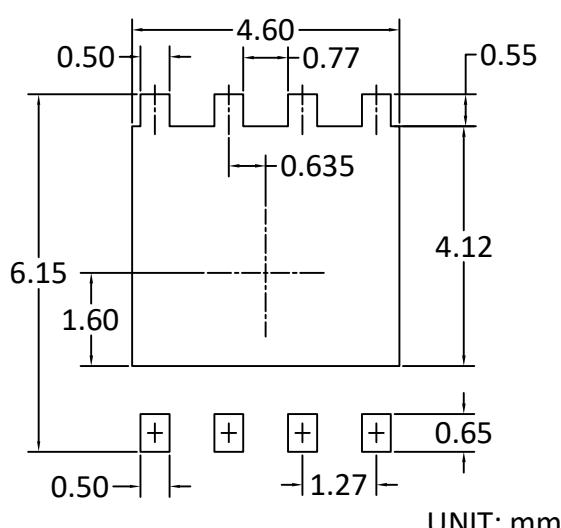


BOTTOM VIEW



VIEW 'A'
(SCALE 5:1)

RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	-	0.05	0.000	-	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.10	5.20	5.30	0.201	0.205	0.209
D1	4.25	4.35	4.45	0.167	0.171	0.175
E	5.45	5.55	5.65	0.215	0.219	0.222
E1	5.95	6.05	6.15	0.234	0.238	0.242
E2	3.525	3.625	3.725	0.139	0.143	0.147
E3	1.175	1.275	1.375	0.046	0.050	0.054
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0.00	-	0.15	0.000	-	0.006
L2	0.68 REF			0.027 REF		
θ	0°	-	10°	0°	-	10°

UNIT: mm

NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
3. THIS PACKAGE WAS QUALIFIED USING IR REFLOW PROCESS (JEDEC STANDARD). FOR USAGE
IN OTHER SOLDERING PROCESSES, PLEASE CONTACT LOCAL AOS REPRESENTATIVES.



ALPHA & OMEGA
SEMICONDUCTOR

**AOS Semiconductor
Product Reliability Report**

AONS66923, rev A

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

May, 2018



This AOS product reliability report summarizes the qualification result for AONS66923. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AONS66923 passes AOS quality and reliability requirements. The released product will be categorized by the process family and be routine monitored for continuously improving the product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Total Sample Size	Number of Failures	Reference Standard
HTGB	Temp = 150°C , Vgs=100% of Vgsmax	168 / 500 / 1000 hours	231 pcs	0	JESD22-A108
HTRB	Temp = 150°C , Vds=100% of Vdsmax	168 / 500 / 1000 hours	231 pcs	0	JESD22-A108
Precondition (Note A)	168hr 85°C / 85%RH + 3 cycle reflow@260°C (MSL 1)	-	4620 pcs	0	JESD22-A113
HAST	130°C , 85%RH, 33.3 psia, Vds = 80% of Vdsmax up to 42V	96 hours	693 pcs	0	JESD22-A110
H3TRB	85°C , 85%RH, Vds = 80% of Vdsmax	1000 hours	693 pcs	0	JESD22-A101
Autoclave	121°C , 29.7psia, RH=100%	96 hours	924 pcs	0	JESD22-A102
Temperature Cycle	-65°C to 150°C , air to air,	1000cycles	924 pcs	0	JESD22-A104
HTSL	Temp = 150°C	1000 hours	693 pcs	0	JESD22-A103
IOL	Δ Tj = 100°C	15000 cycles	693 pcs	0	AEC Q101

Note: The reliability data presents total of available generic data up to the published date.

Note A: MSL (Moisture Sensitivity Level) 1 based on J-STD-020

II. Reliability Evaluation

FIT rate (per billion): 7.63

MTTF = 14960 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

$$\text{Failure Rate} = \text{Chi}^2 \times 10^9 / [2 (N) (H) (Af)] = 7.63$$

$$\text{MTTF} = 10^9 / \text{FIT} = 14960 \text{ years}$$

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval

N = Total Number of units from burn-in tests

H = Duration of burn-in testing

Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)

Acceleration Factor [**Af**] = $\text{Exp} [Ea / k (1/T_j u - 1/T_j s)]$

Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	259	87	32	13	5.64	2.59	1

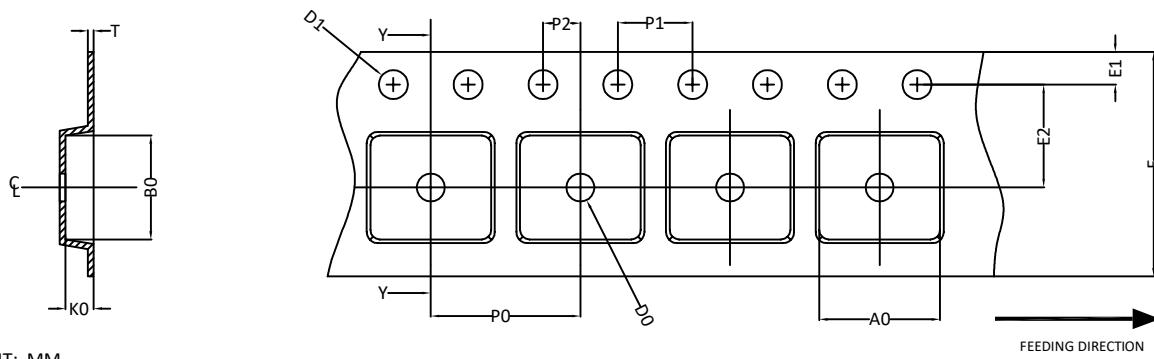
T_j s = Stressed junction temperature in degree (Kelvin), K = C+273.16

T_j u = The use junction temperature in degree (Kelvin), K = C+273.16

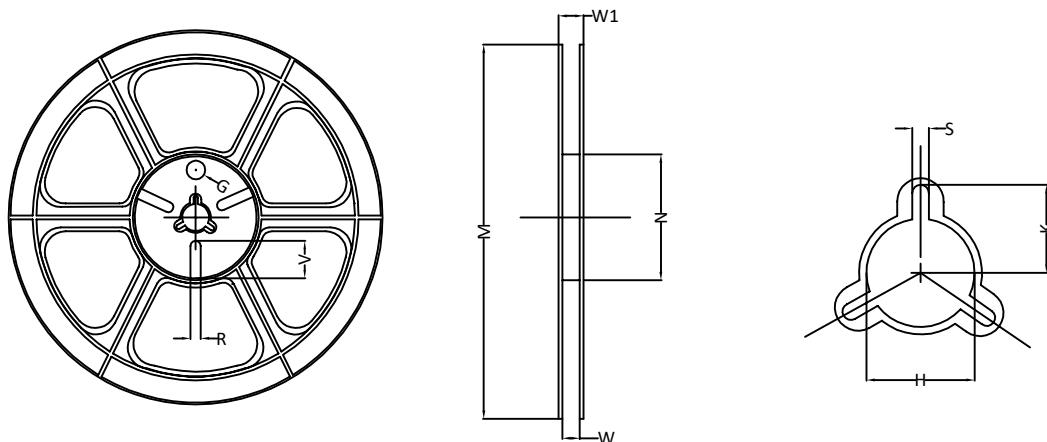
k = Boltzmann's constant, 8.617164 X 10⁻⁵eV / K



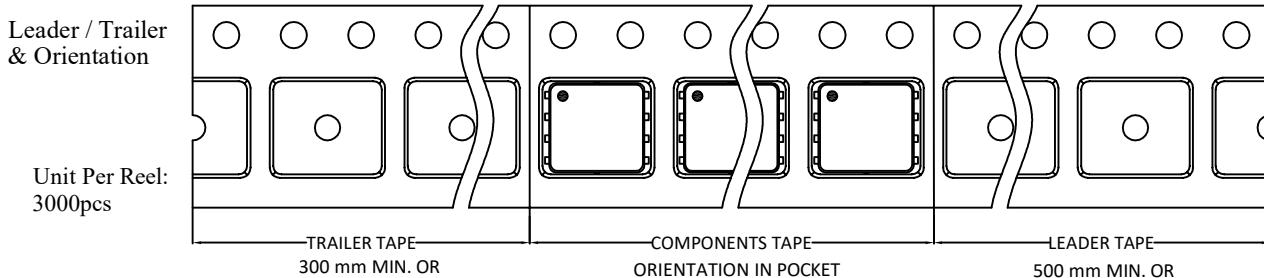
DFN5x6 Carrier Tape



DFN5x6 Reel



DFN5x6 Punch Package Tape



DFN5x6 Sawing Package (Except DFN5x6 7L EP1 TEP1 S/DFN5x6 2L EP3 TEP1 S/ /DFN5x6 8L EP1 TEP1 S/DFN5x6 8L EP1 TEP2 S/DFN5x6 8L EP2 TEP1 S/ DFN5x6A 8L EP2 TEP1 S) Tape

