



**General Description**

The AOD603A uses advanced trench technology MOSFETs to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

**Product Summary**

**N-Channel**

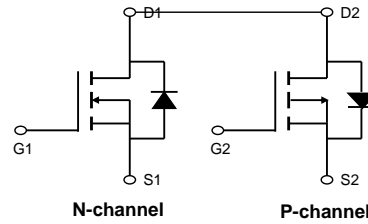
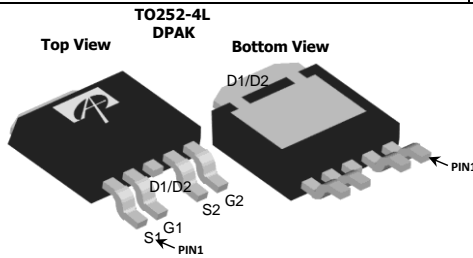
$V_{DS} = 60V$   
 $I_D = 13A$  ( $V_{GS} = 10V$ , silicon limit)  
 $R_{DS(ON)} < 60m\Omega$  ( $V_{GS} = 10V$ )  
 $< 85m\Omega$  ( $V_{GS} = 4.5V$ )

100% UIS Tested  
 100%  $R_g$  Tested

**P-Channel**

$-60V$   
 $-13A$  ( $V_{GS} = -10V$ , silicon limit)  
 $R_{DS(ON)} < 115m\Omega$  ( $V_{GS} = -10V$ )  
 $< 150m\Omega$  ( $V_{GS} = -4.5V$ )

100% UIS Tested  
 100%  $R_g$  Tested



**Absolute Maximum Ratings  $T_A = 25^\circ C$  unless otherwise noted**

Parameter	Symbol	Max N-channel	Max P-channel	Units	
Drain-Source Voltage	$V_{DS}$	60	-60	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V	
Continuous Drain Current	$I_D$	$T_C = 25^\circ C$ (silicon limit)	13.6	-13.4	A
		$T_C = 25^\circ C^G$	12	-12	
		$T_C = 100^\circ C$	9.5	-9.5	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	30	-30		
Continuous Drain Current	$I_{DSM}$	$T_A = 25^\circ C$	3.5	-3	A
		$T_A = 70^\circ C$	3	-2.5	
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	19	25	A	
Avalanche energy $L = 0.1mH$ <sup>C</sup>	$E_{AS}, E_{AR}$	18	31	mJ	
Power Dissipation <sup>B</sup>	$P_D$	$T_C = 25^\circ C$	27	42.5	W
		$T_C = 100^\circ C$	13.5	21.5	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A = 25^\circ C$	2	2	W
		$T_A = 70^\circ C$	1.3	1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	-55 to 175	$^\circ C$	

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
<b>Parameter N-channel</b>				
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	19	23	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		50	60	$^\circ C/W$
Maximum Junction-to-Case		$R_{\theta JC}$	4	5.5
<b>Parameter P-channel</b>				
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	19	23	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		50	60	$^\circ C/W$
Maximum Junction-to-Case		$R_{\theta JC}$	2.5	3.5

**N-Channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	1	2.4	3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =12A T <sub>J</sub> =125°C		47 90	60 110	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A		67	85	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =12A		22		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.74	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				12	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =30V, f=1MHz		450		pF
C <sub>oss</sub>	Output Capacitance			61		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			27		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.6	1.35	2	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =12A		7.5	12	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			3.8	7	nC
Q <sub>gs</sub>	Gate Source Charge			1.2		nC
Q <sub>gd</sub>	Gate Drain Charge			1.9		nC
t <sub>D(on)</sub>	Turn-On DelayTime			4.2		ns
t <sub>r</sub>	Turn-On Rise Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, R <sub>L</sub> =2.5Ω,		3.4		ns
t <sub>D(off)</sub>	Turn-Off DelayTime	R <sub>GEN</sub> =3Ω		16		ns
t <sub>f</sub>	Turn-Off Fall Time			2		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =12A, di/dt=100A/μs		27		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =12A, di/dt=100A/μs		30		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175° C. The SOA curve provides a single pulse rating.

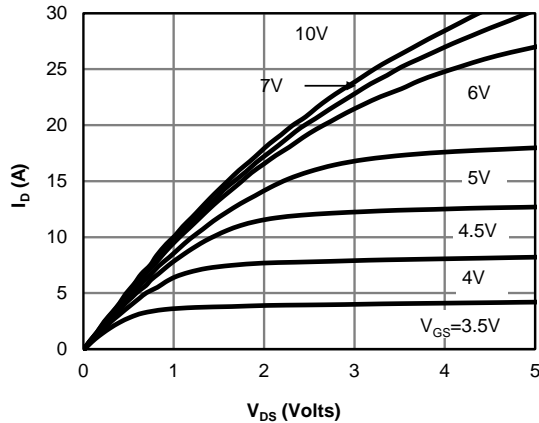
G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

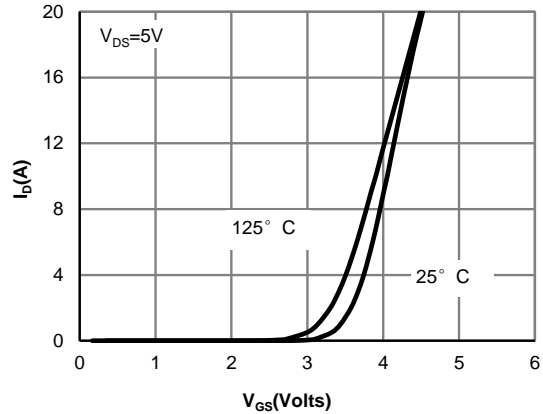
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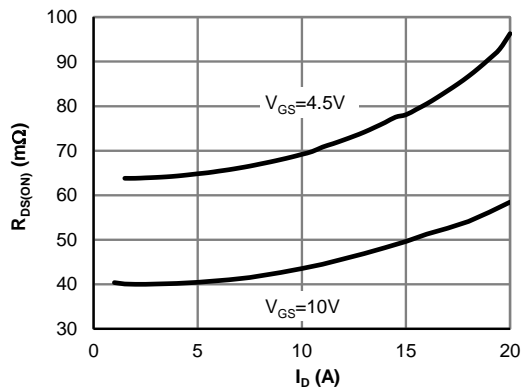
**N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



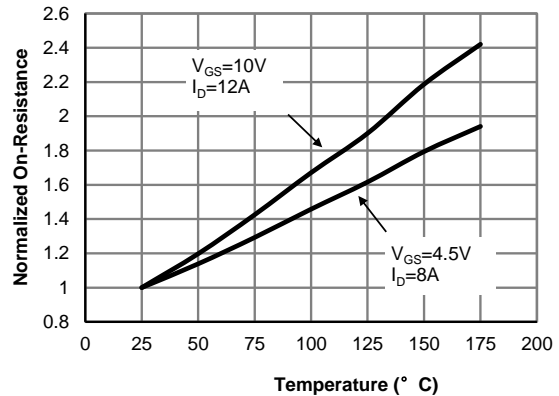
**Fig 1: On-Region Characteristics (Note E)**



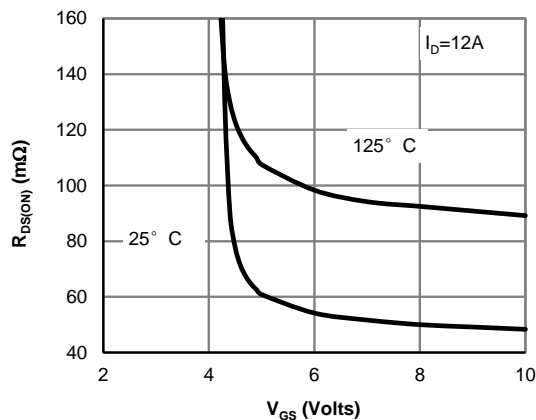
**Figure 2: Transfer Characteristics (Note E)**



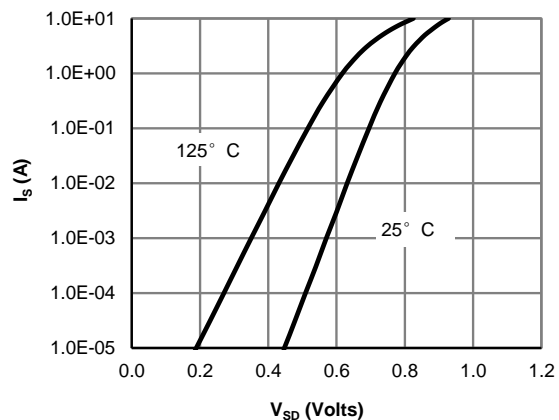
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

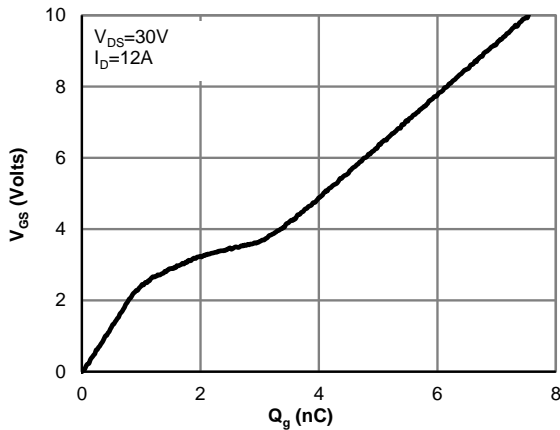


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

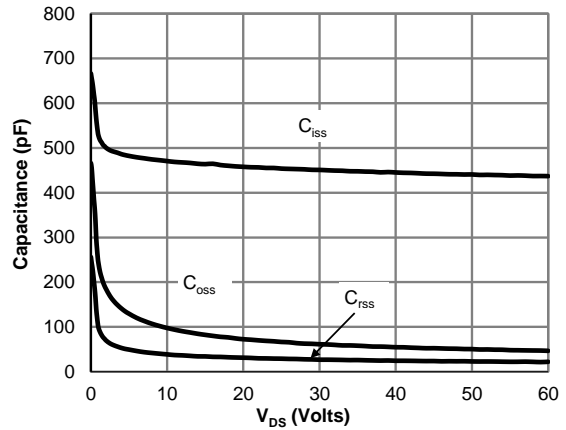


**Figure 6: Body-Diode Characteristics (Note E)**

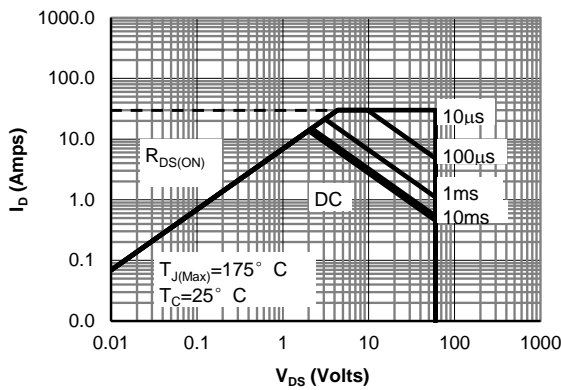
**N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



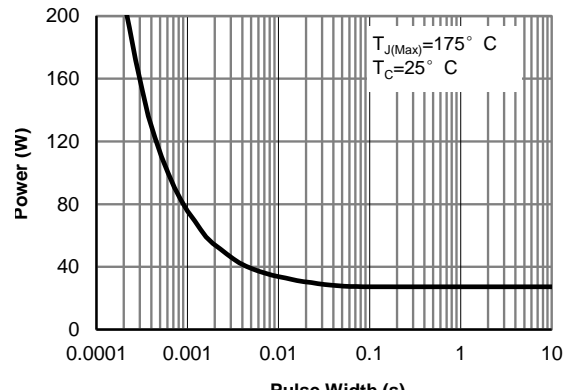
**Figure 7: Gate-Charge Characteristics**



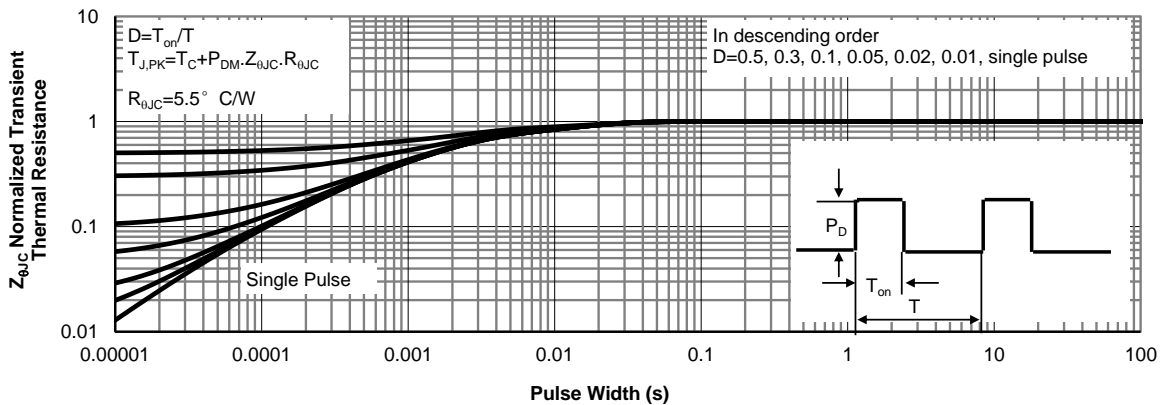
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

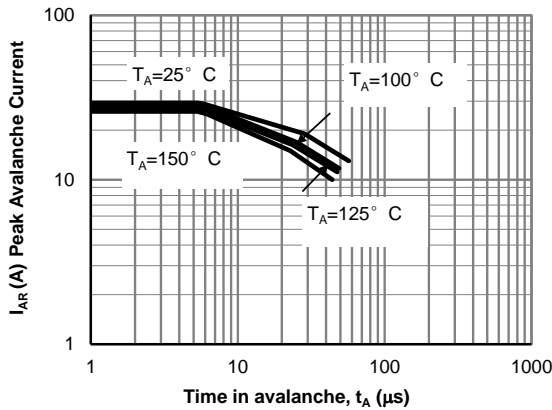


**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

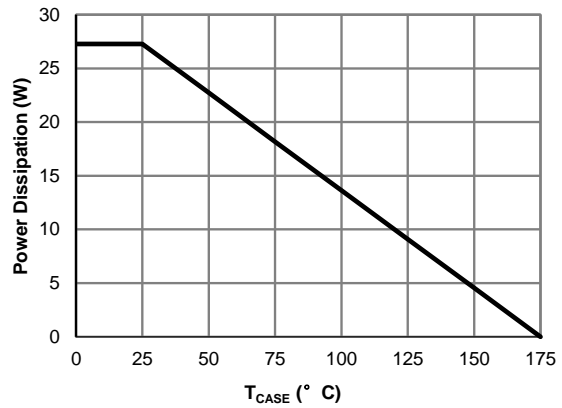


**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

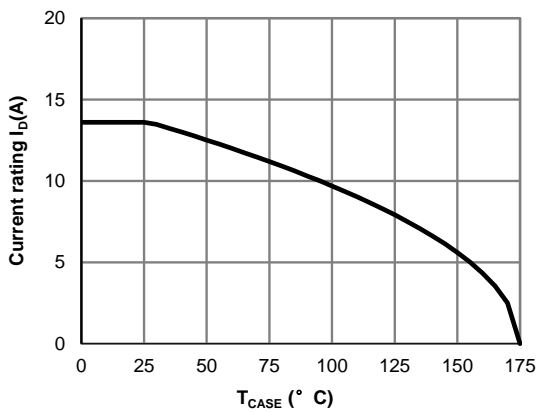
**N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



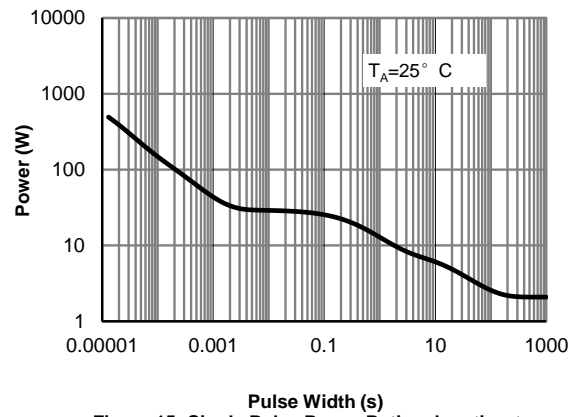
**Figure 12: Single Pulse Avalanche capability (Note C)**



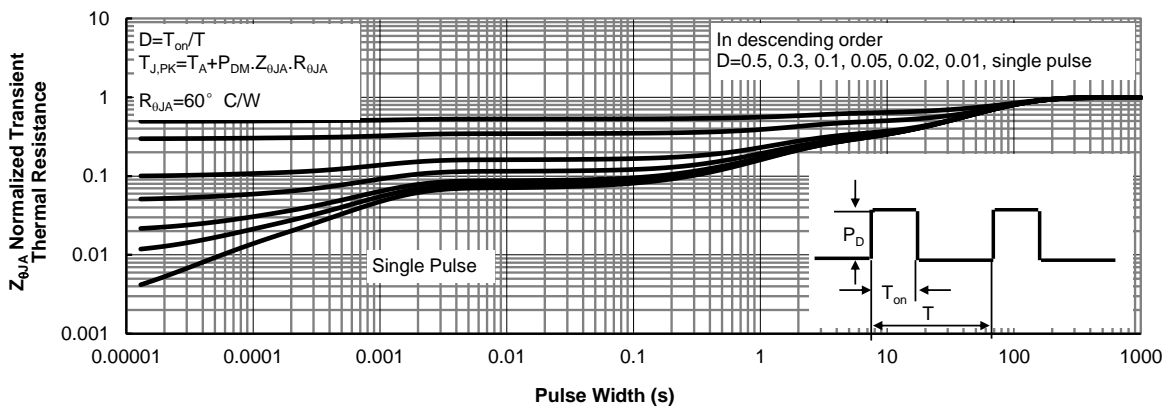
**Figure 13: Power De-rating (Note F)**



**Figure 14: Current De-rating (Note F)**

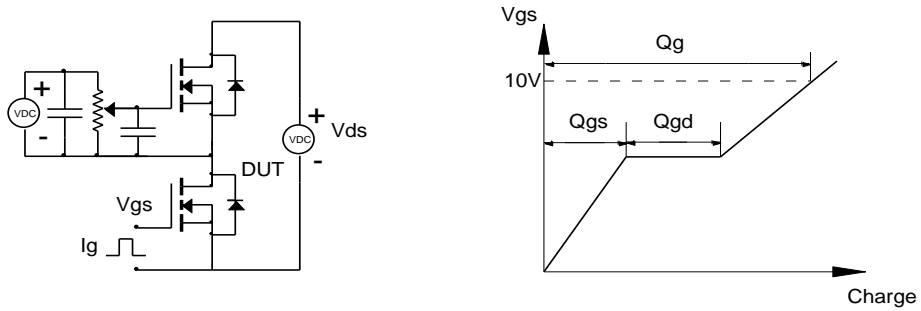


**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

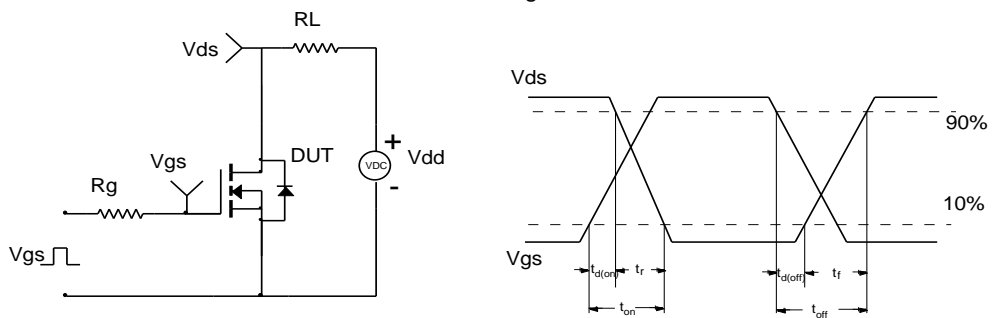


**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

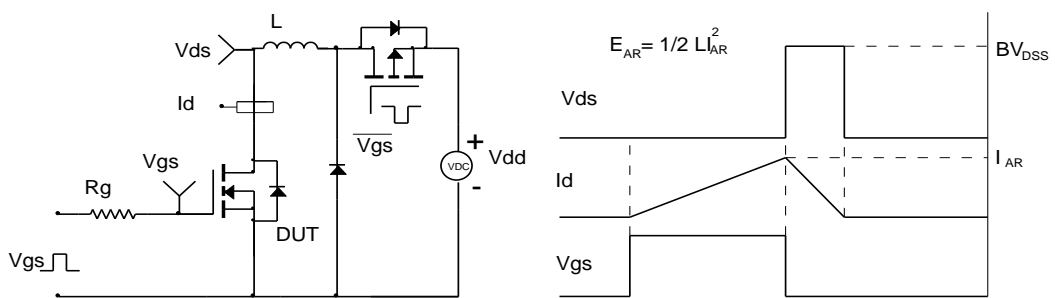
**Gate Charge Test Circuit & Waveform**



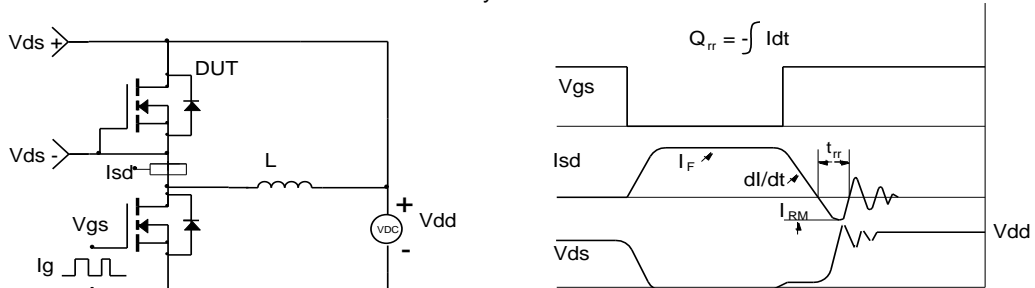
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**P-Channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =-250μA	-1.5	-2.1	-3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-12A T <sub>J</sub> =125°C		91	115	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-8A		150	180	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-12A		12		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.76	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				-12	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-30V, f=1MHz		960		pF
C <sub>oss</sub>	Output Capacitance			86		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			38		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		9.5	15	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-30V, I <sub>D</sub> =-12A		15.8	22	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			7.4	12	nC
Q <sub>gs</sub>	Gate Source Charge			3		nC
Q <sub>gd</sub>	Gate Drain Charge			3.5		nC
t <sub>D(on)</sub>	Turn-On DelayTime			9		ns
t <sub>r</sub>	Turn-On Rise Time	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-30V, R <sub>L</sub> =2.5Ω,		10		ns
t <sub>D(off)</sub>	Turn-Off DelayTime	R <sub>GEN</sub> =3Ω		25		ns
t <sub>f</sub>	Turn-Off Fall Time			11		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-12A, dI/dt=100A/μs		27.5		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-12A, dI/dt=100A/μs		30		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175° C. The SOA curve provides a single pulse rating.

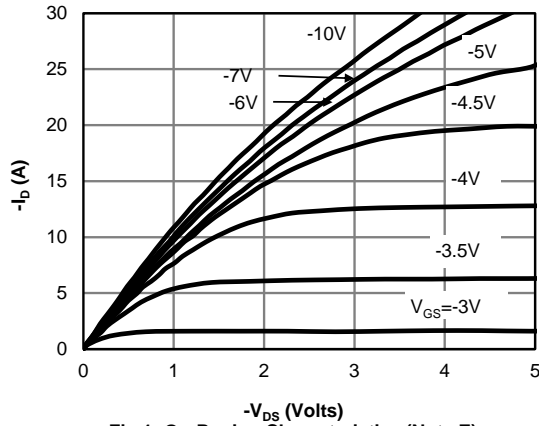
G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

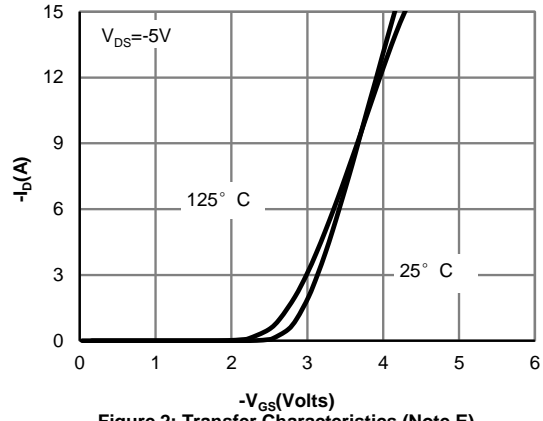
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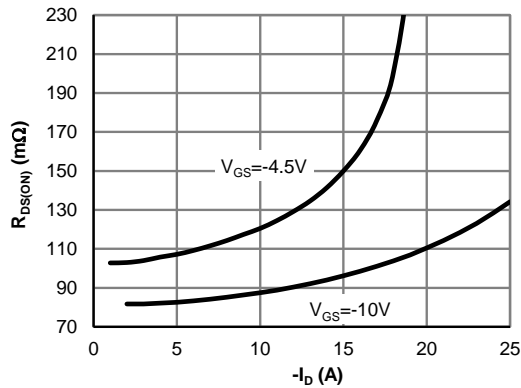
**P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



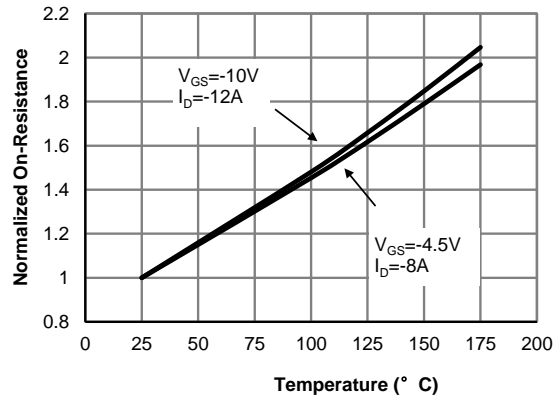
**Fig 1: On-Region Characteristics (Note E)**



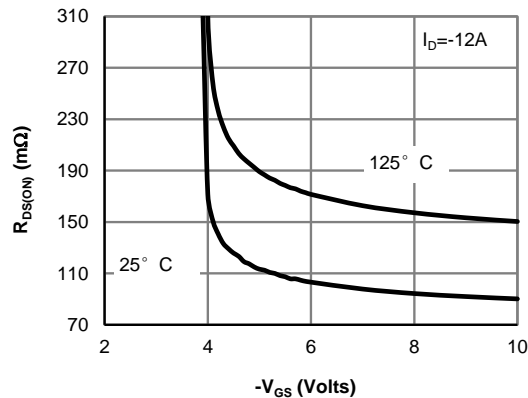
**Figure 2: Transfer Characteristics (Note E)**



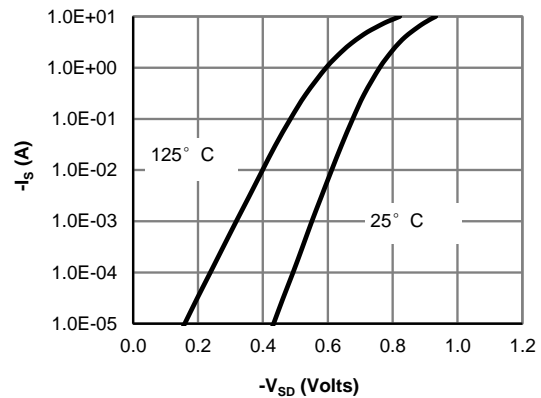
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**



**Figure 6: Body-Diode Characteristics (Note E)**



**P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

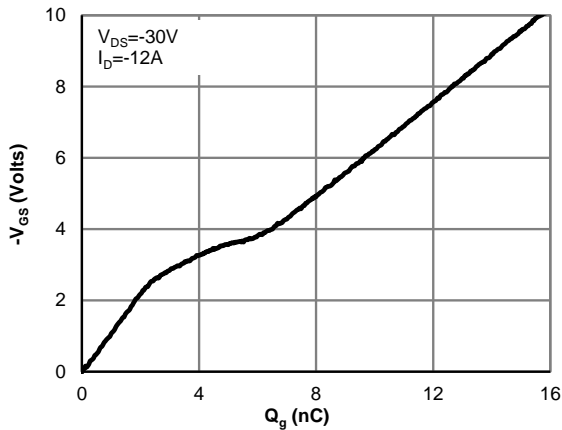


Figure 7: Gate-Charge Characteristics

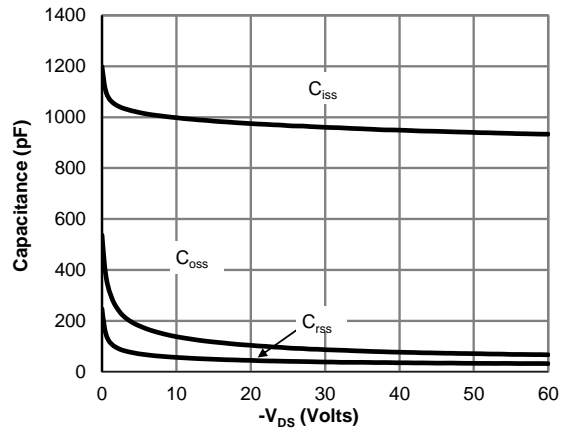


Figure 8: Capacitance Characteristics

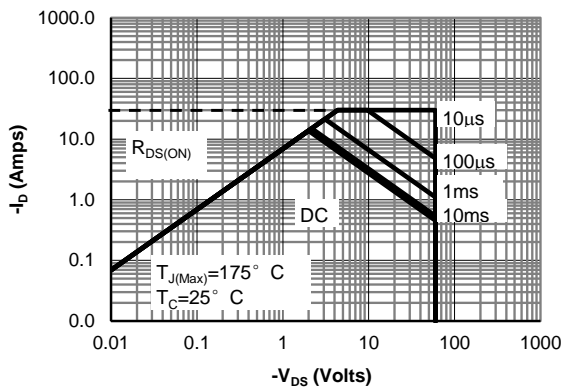


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

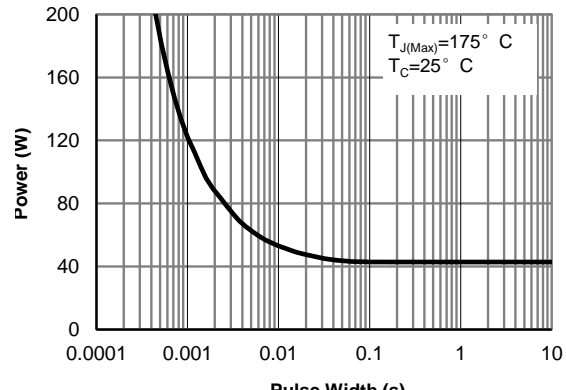


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

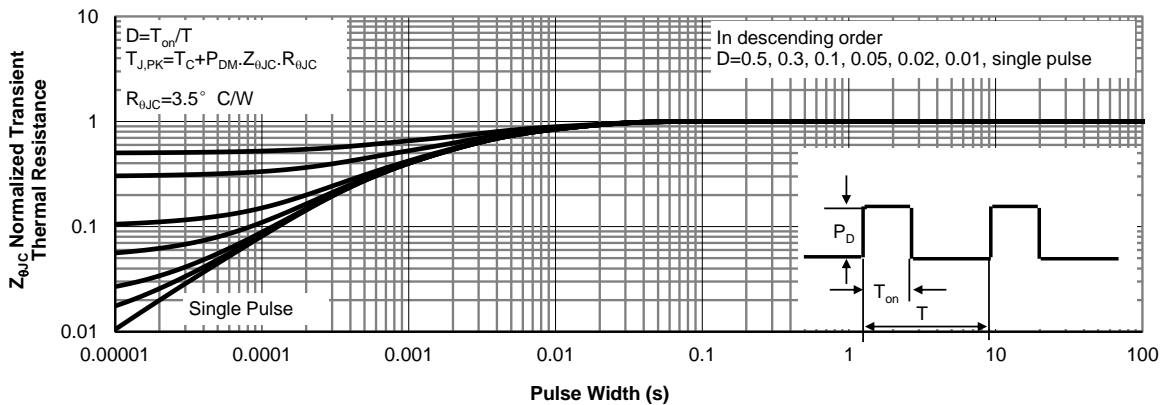
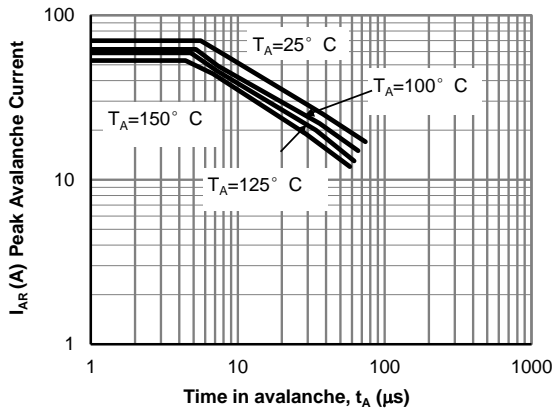
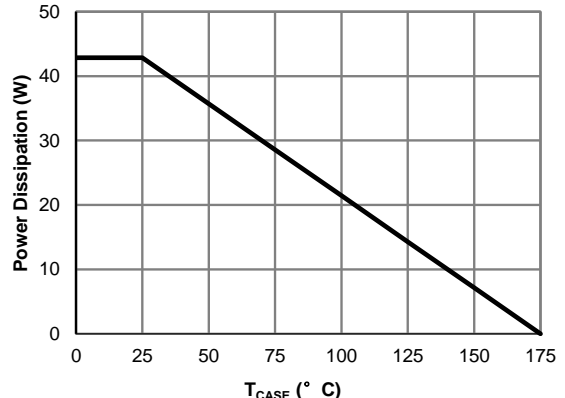


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

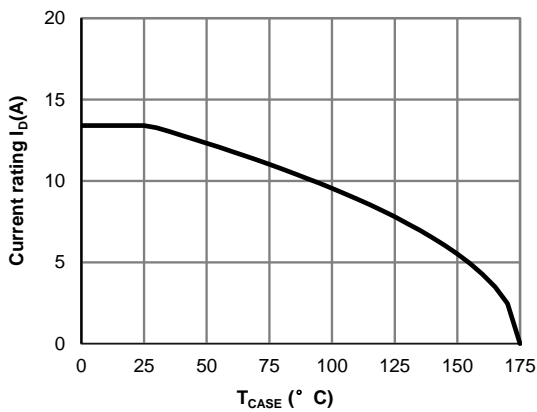
**P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



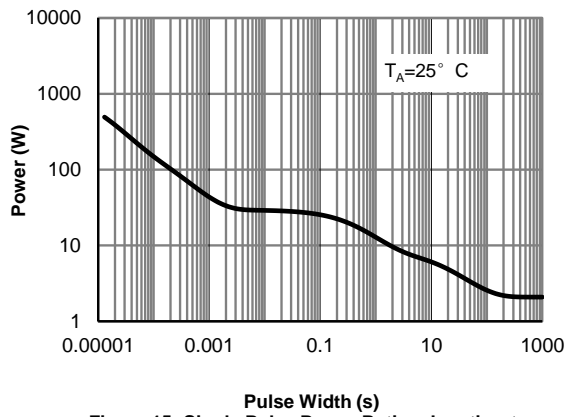
**Figure 12: Single Pulse Avalanche capability (Note C)**



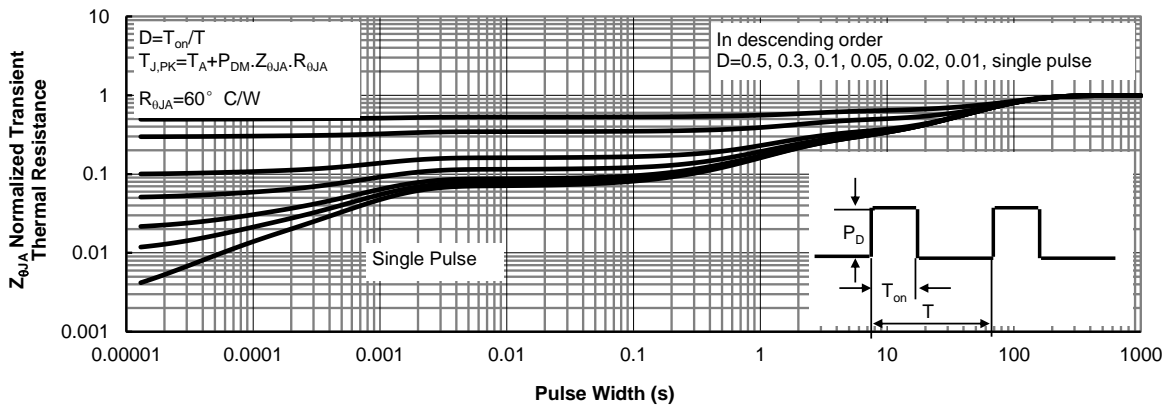
**Figure 13: Power De-rating (Note F)**



**Figure 14: Current De-rating (Note F)**

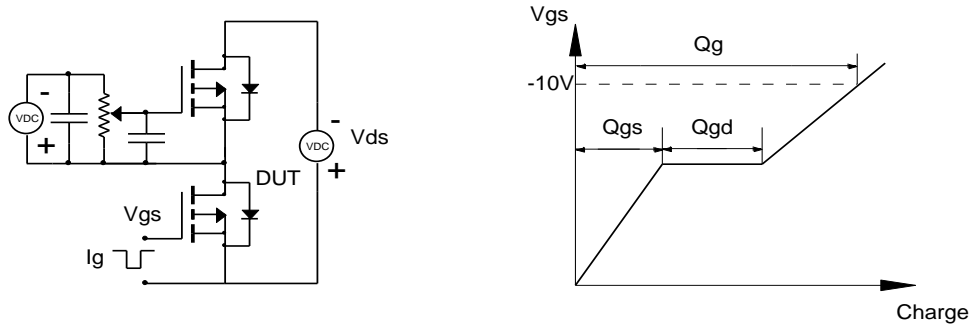


**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

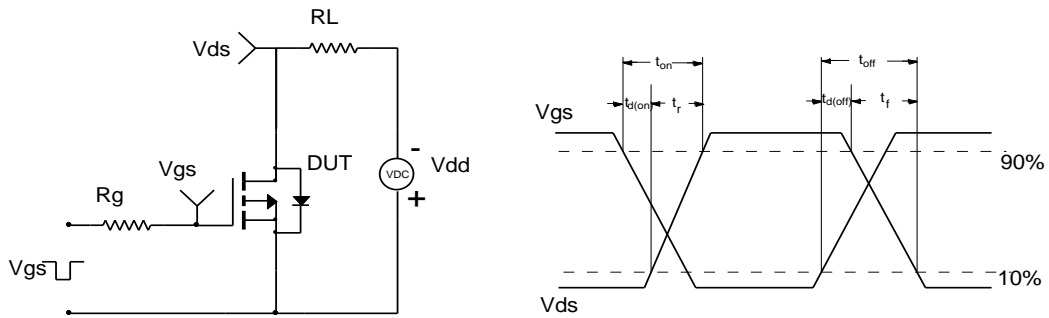


**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

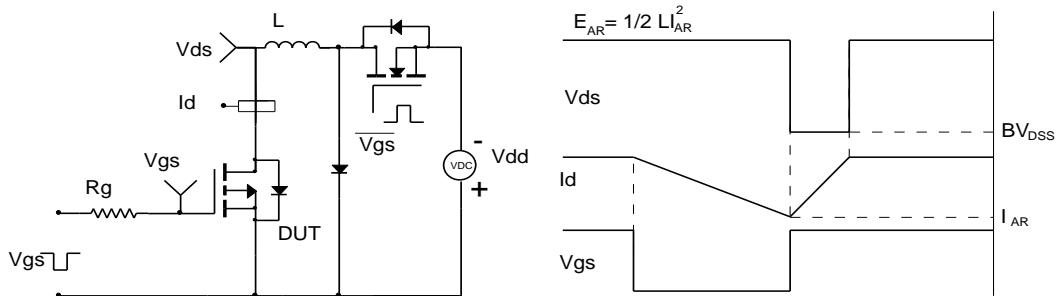
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

