AOZ8809DI

Ultra-Low Capacitance TVS Diode

General Description

The AOZ8809DI is a transient voltage suppressor array designed to protect high speed data lines such as HDMI 1.4/2.0, USB 3.0/3.1, MDDI, SATA, and Gigabit Ethernet from damaging ESD events.

This device incorporates eight surge rated, low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground.

The AOZ8809DI provides a typical line-to-line capacitance of 0.25 pF and low insertion loss up to 6 GHz providing greater signal integrity making it ideally suited for
HDMI 1.4/2.0 or USB 3.0/3.1 applications, such as Digital TVs, DVD players, computing, set-top boxes and MDDI applications in mobile computing devices.

The AOZ8809DI comes in a RoHS compliant and Halogen Free 2.5 mm x 1.0 mm x 0.55 mm DFN-10 package and is rated for -40 °C to +85 °C junction temperature range.

Features

- ESD protection for high-speed data lines:
  - IEC 61000-4-2, level 4 (ESD) immunity test
  - Air discharge: ±15 kV; contact discharge: ±15 kV
  - IEC61000-4-4 (EFT) 40 A (5/50 nS)
  - IEC61000-4-5 (Lightning) 4 A (8/20 µS)
  - Human Body Model (HBM) ±24 kV
- Array of surge rated diodes with internal TVS diode
- Small package saves board space
- Protects four I/O lines
- Low capacitance between I/O lines: 0.25 pF
- Low clamping voltage
- Low operating voltage: 3.3V, 5.0 V

Applications

- HDMI 1.4/2.0, USB 3.0/3.1, MDDI, SATA ports
- Monitors and flat panel displays
- Set-top box
- Video graphics cards
- Digital Video Interface (DVI)
- Notebook computers

Green Product

Typical Applications

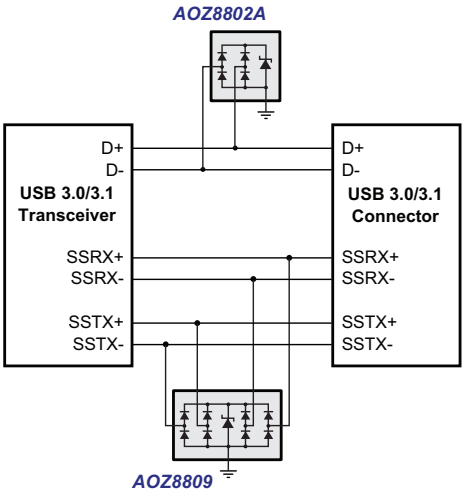


Figure 1. USB 3.0/3.1 Ports

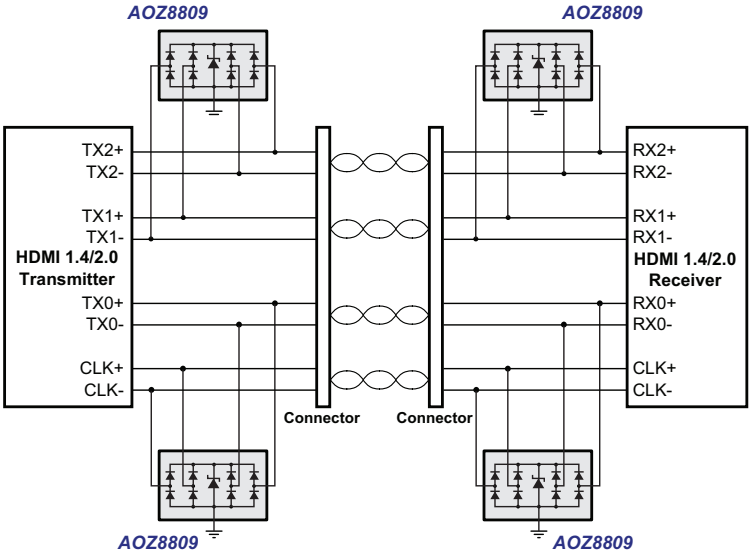


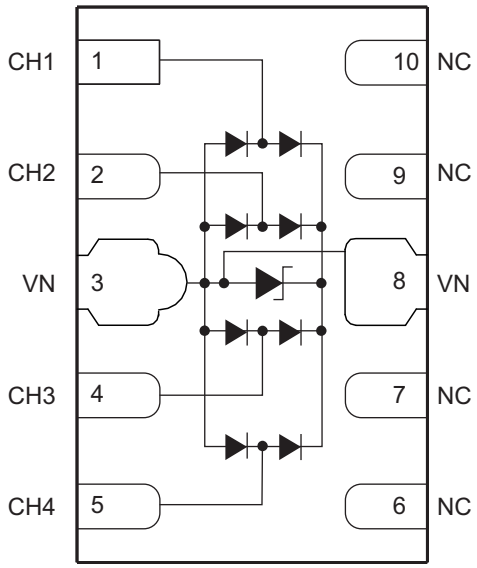
Figure 2. HDMI 1.4/2.0 Ports

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8809DI-03	-40 °C to +85 °C	2.5 mm x 1.0 mm x 0.55 mm DFN-10	Green Product
AOZ8809DI-05			

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



DFN-10
(Top View)

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	AOZ8809DI-03	AOZ8809DI-05
Storage Temperature (T_S)	-65 °C to +150 °C	
ESD Rating per IEC61000-4-2, contact(1)(3)	±15 kV	
ESD Rating per IEC61000-4-2, air(1)(3)	±15 kV	
ESD Rating per Human Body Model(2)(3)	±24 kV	

Notes:

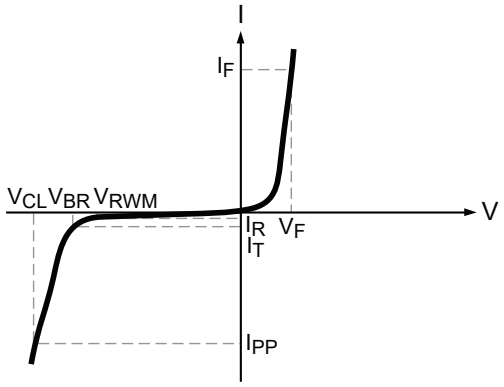
1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330 Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100 pF, $R_{Discharge}$ = 1.5 kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40 °C to +125 °C

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Diagram
I_{PP}	Maximum Reverse Peak Pulse Current	
V_{CL}	Clamping Voltage @ I_{PP} 100ns Transmission Line Pulse (TLP)	
V_{ESD}	ESD Clamping Voltage (IEC61000-4-2 +6kV Contact Discharge)	
V_{RWM}	Working Peak Reverse Voltage	
I_R	Maximum Reverse Leakage Current	
V_{BR}	Breakdown Voltage	
I_T	Test Current	
V_F	Forward Voltage @ I_F	
C_J	Max. Capacitance @ V_R = 0 and f = 1 MHz	

Device	Device Marking	V_{RWM} (V) Max.	V_{BR} (V) Min. I_T = 100 µA	I_R (µA) Max.	V_F (V) Typ.	V_{CL} Max.(3)		V_{ESD} (V)(3)	C_J (pF)(3,4)	
						I_{PP} = 2 A	I_{PP} = 12 A	Typ.	Typ.	Max.
AOZ8809DI-03	H	3.3	3.5	1.0	0.85	3.5	8.0	8.0	0.45	0.6
AOZ8809DI-05	K	5.0	6.0	1.0	0.85	4.0	9.0	8.0	0.45	0.6

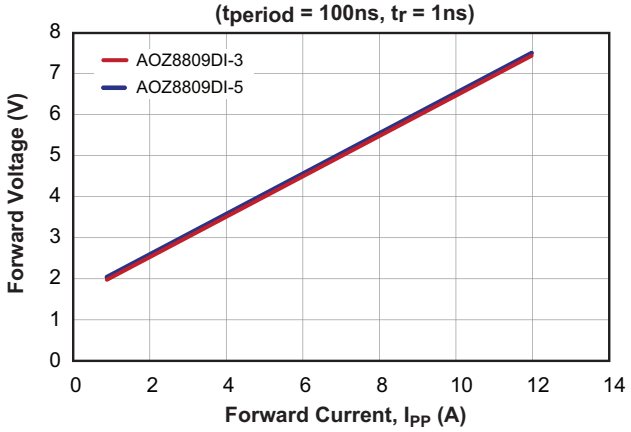
Notes:

3. These specifications are guaranteed by design and characterization.

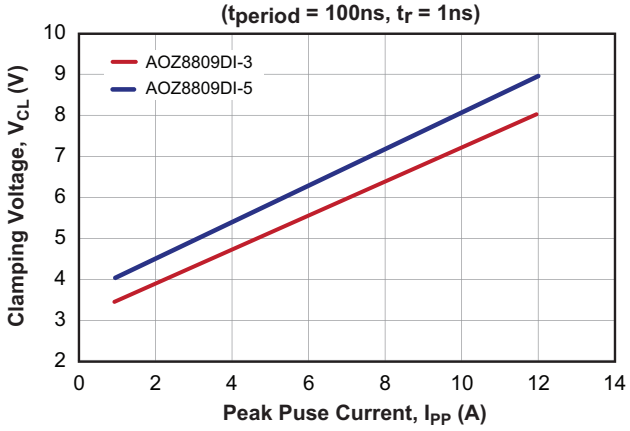
4. V_{PIN} 3,8 = 0V, V_{IN} = 2.5V, f = 1MHz, T = 25°C, any I/o pin to Ground.

Typical Performance Characteristics

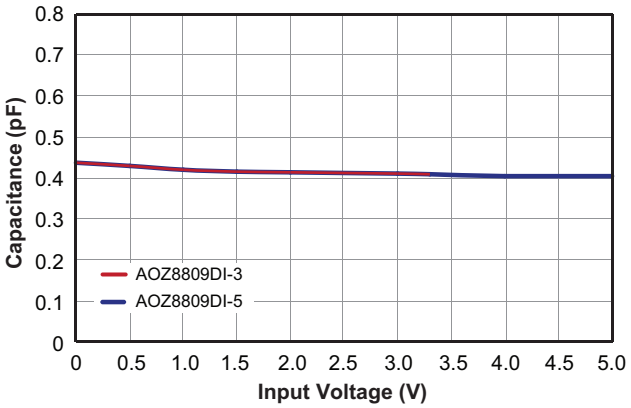
Forward Voltage vs. Forward Peak Pulse Current
(t_{period} = 100ns, t_r = 1ns)



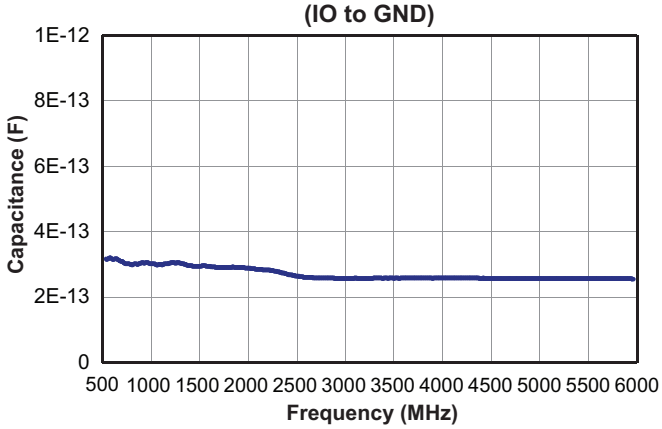
Clamping Voltage vs. Peak Pulse Current
(t_{period} = 100ns, t_r = 1ns)



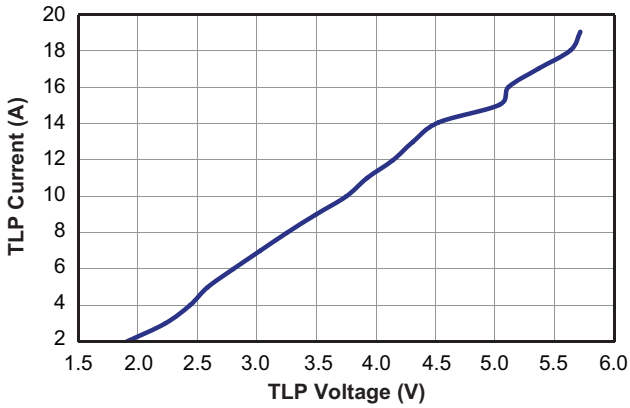
Typical Variation of CIN vs. VIN



Capacitance vs. Frequency
(IO to GND)

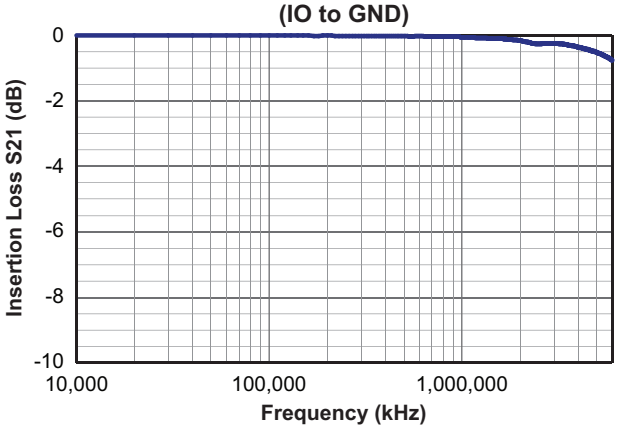


Transmission Line Pulsing (TLP) Measurement

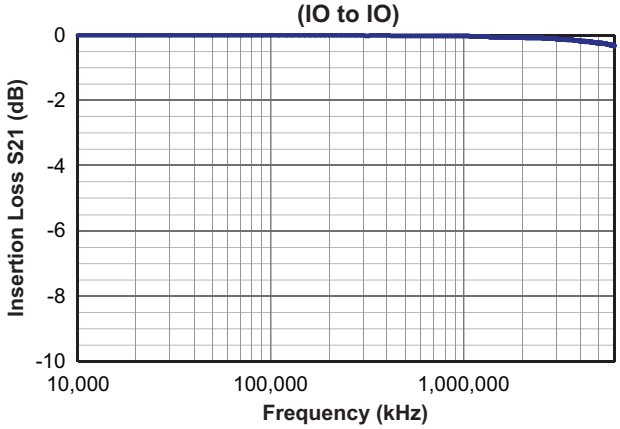


Typical Performance Characteristics *(Continued)*

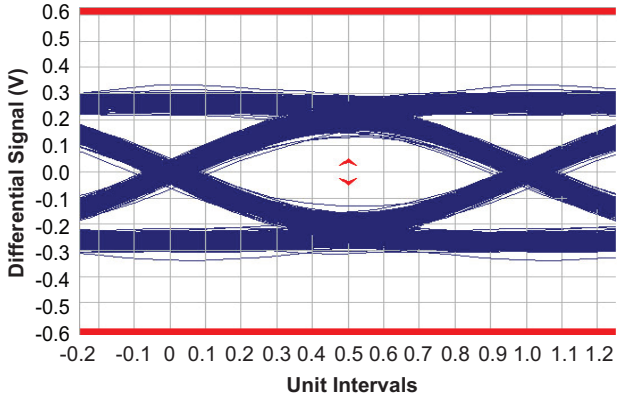
Insertion Loss vs. Frequency (IO to GND)



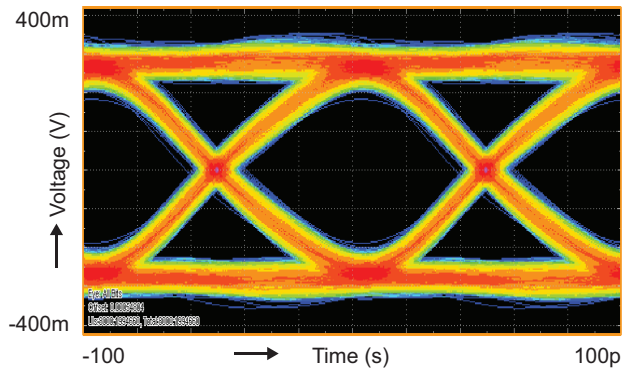
Insertion Loss vs. Frequency (IO to IO)



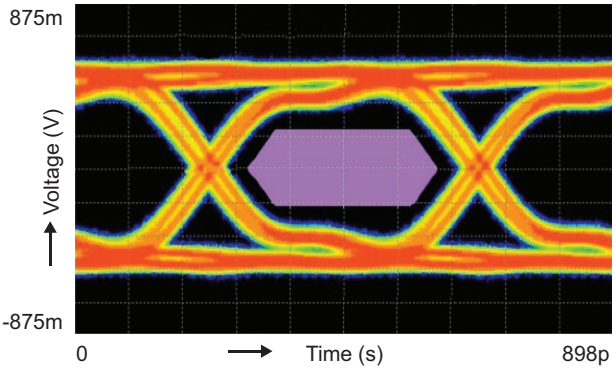
USB 3.0 Eye Diagram with AOZ8809 (5Gbps)



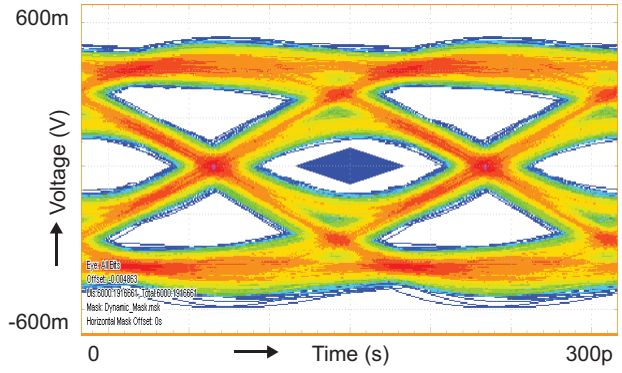
USB 3.1 Eye Diagram with AOZ8809 (10Gbps)



HDMI 1.4 Eye Diagram with AOZ8809



HDMI 2.0 Eye Diagram with AOZ8809



High Speed PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8809DI devices should be located as close as possible to the noise source. The AOZ8809DI device should be placed on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8809DI devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8809DI device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design.

The AOZ8809DI ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. The AOZ8809DI is designed for ease of PCB layout by allowing the traces to run underneath the device. The pinout of the AOZ8809DI is designed to simply drop onto the IO lines of a High Definition Multimedia Interface (HDMI 1.4/2.0) or USB 3.0/3.1 design without having to divert the signal lines that may add more parasitic inductance. Pins 1, 2, 4 and 5 are connected to the internal TVS devices and pins 6, 7, 9 and 10 are no connects. The no connects was done so the package can be securely soldered onto the PCB surface.

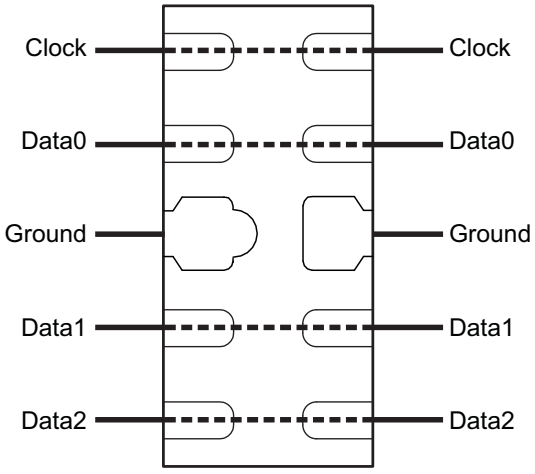


Figure 3. Flow Through Layout for HDMI 1.4/2.0

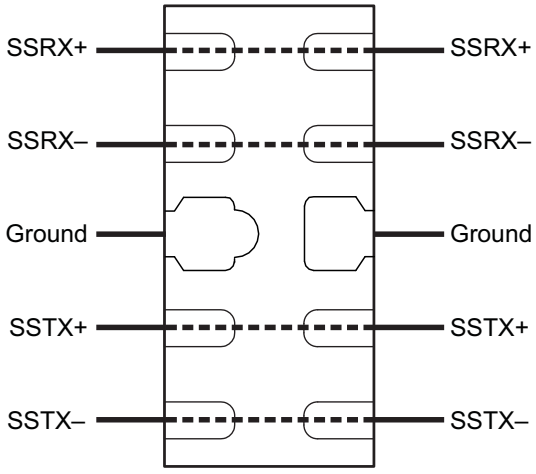


Figure 4. Flow Through Layout for USB 3.0/3.1

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Document No.	PD-02091
Version	A
Title	AOZ8809DI-05 Marking Description

DFN2.5X1.0 Power IC PACKAGE MARKING DESCRIPTION



Green product

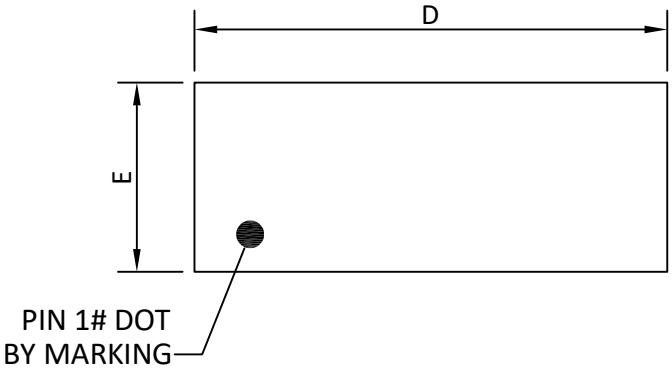
NOTE:
P - Part number code
W - Week code and year code
L&T - Assembly lot code & Assembly location code

PART NO.	DESCRIPTION	CODE
AOZ8809DI-05	Green product	K

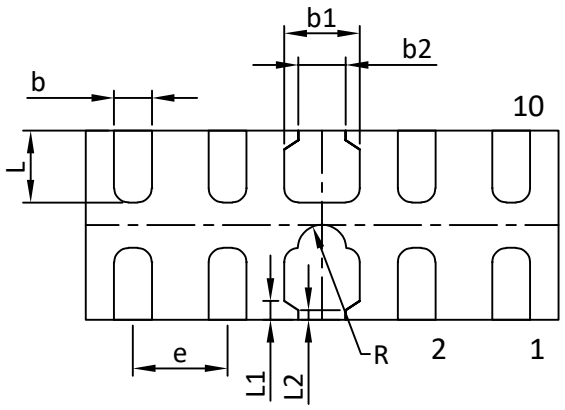
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Document No.	PO-00078
Version	I

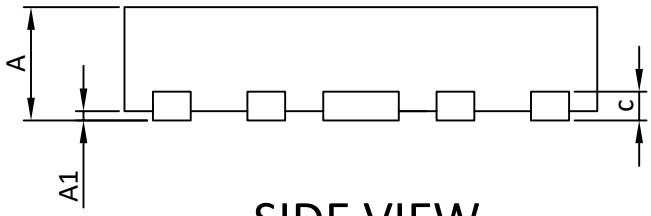
DFN2.5x1.0_10L_EP2_S PACKAGE OUTLINE



TOP VIEW

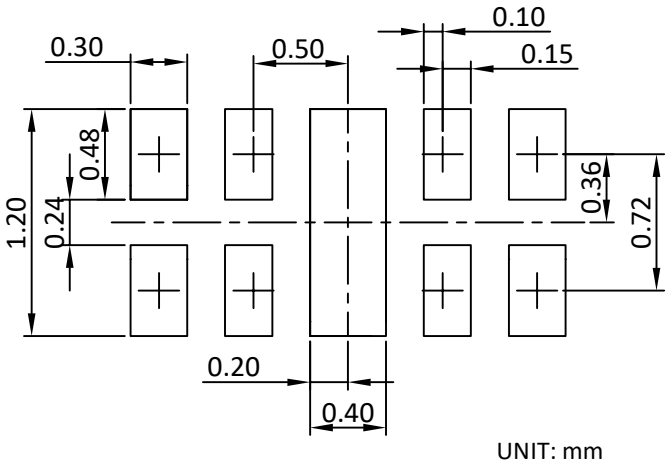


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.525	0.60	0.018	0.021	0.024
A1	0.00	---	0.05	0.000	----	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	---	0.40	---	----	0.016	----
b2	---	0.25	---	----	0.010	----
c	0.152 REF			0.006 REF		
D	2.45	2.50	2.55	0.096	0.098	0.100
e	0.50 BSC			0.020 BSC		
E	0.95	1.00	1.05	0.037	0.039	0.041
L	0.33	0.38	0.43	0.013	0.015	0.017
L1	0.075 REF			0.003 REF		
L2	0.05 REF			0.002 REF		
R	0.13 REF			0.005 REF		

NOTE:

1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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AOS Semiconductor
Product Reliability Report

AOZ8809DI-05, rev B

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

Jan. 2018

ALPHA & OMEGA SEMICONDUCTOR

This AOS product reliability report summarizes the qualification result for AOZ8809DI-05. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AOZ8809DI-05 passes AOS quality and reliability requirements. The released product will be categorized by the process family and be routine monitored for continuously improving the product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Total Sample Size	Number of Failures	Reference Standard
HTRB	**Temp = 150°C , Vdd=100% of VRWMmax**	**168 / 500 / 1000 hours**	**462 pcs**	**0**	**JESD22-A108**
Precondition (Note A)	**168hr 85°C / 85%RH + 3 cycle reflow@260°C**	**-**	**1386 pcs**	**0**	**JESD22-A113**
HAST	**130°C , 85%RH, 33.3 psia, Vdd = 80% of VRWMmax**	**96 hours**	**462 pcs**	**0**	**JESD22-A110**
Autoclave	**121°C , 29.7psia, RH=100%**	**96 hours**	**462 pcs**	**0**	**JESD22-A102**
Temperature Cycle	**-65°C to 150°C , air to air**	**250 / 500 cycles**	**462 pcs**	**0**	**JESD22-A104**

Note: The reliability data presents total of available generic data up to the published date.
Note A: MSL (Moisture Sensitivity Level) 1 based on J-STD-020

II. Reliability Evaluation

FIT rate (per billion): 7.63
MTTF = 14960 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $Chi^2 \times 10^9$ **/ [**2 (N) (H) (Af)**] =** 7.63
MTTF = 10^9 / FIT = 14960 years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval
N = Total Number of units from burn-in tests
H = Duration of burn-in testing
Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)
Acceleration Factor [**Af**] = **Exp** [Ea / **k** (1/Tj u – 1/Tj s)]

Acceleration Factor ratio list:

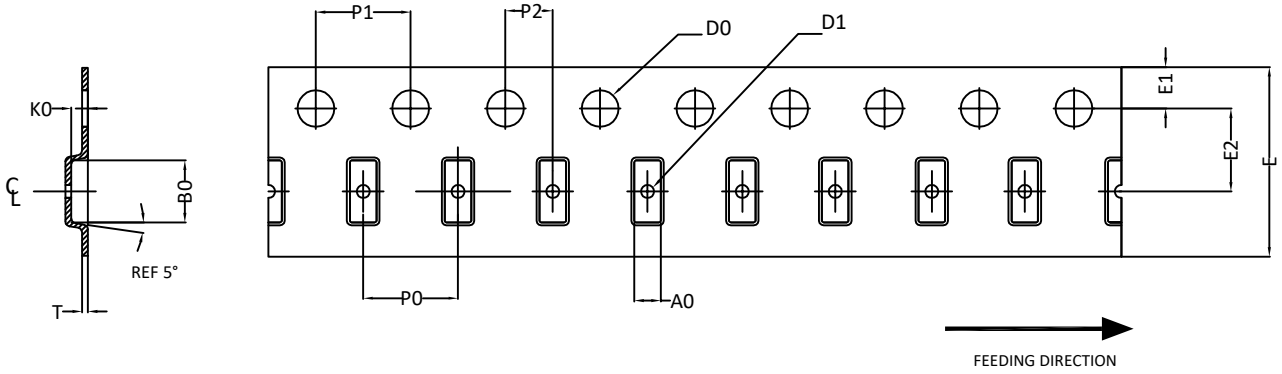
	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	**259**	**87**	**32**	**13**	**5.64**	**2.59**	**1**

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16
Tj u =The use junction temperature in degree (Kelvin), K = C+273.16
k = Boltzmann's constant, 8.617164 X 10^{-5}eV / K

ALPHA & OMEGA SEMICONDUCTOR

DFN2.5x1.0_10L_EP2_S/DFN2.5x1.0A_10L_EP2_S Tape and Reel Data

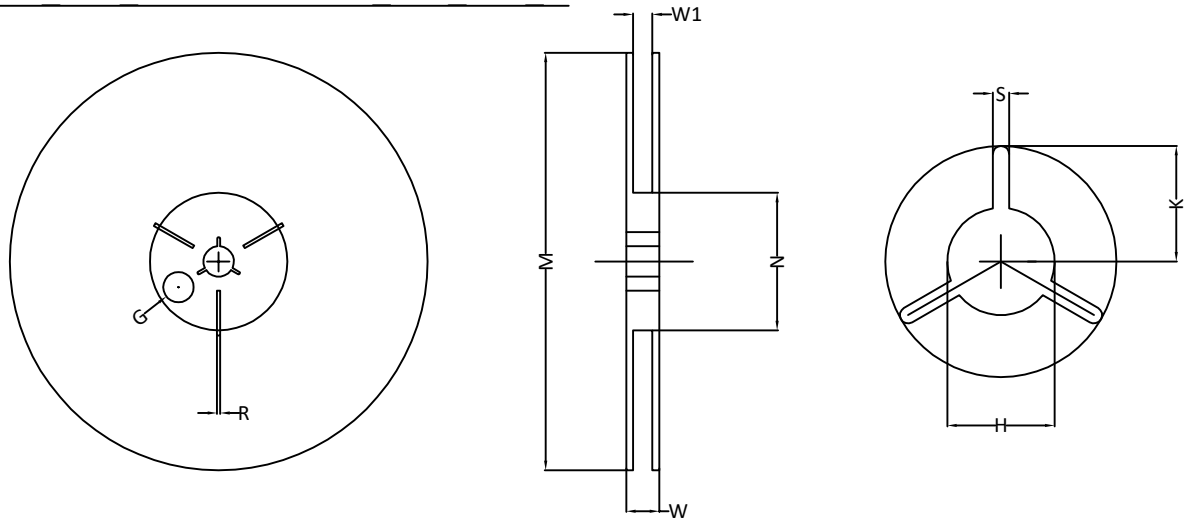
DFN2.5x1.0_10L_EP2_S/DFN2.5x1.0A_10L_EP2_S Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN2.5x1.0(A)	1.12 ±0.05	2.62 ±0.05	0.70 ±0.05	Ø1.55 ±0.05	Ø0.55 ±0.05	8.00 +0.3 -0.1	1.75 ±0.1	3.50 ±0.05	4.00 ±0.1	4.0 ±0.10	2.0 ±0.05	0.25 ±0.05

DFN2.5x1.0_10L_EP2_S/DFN2.5x1.0A_10L_EP2_S Reel



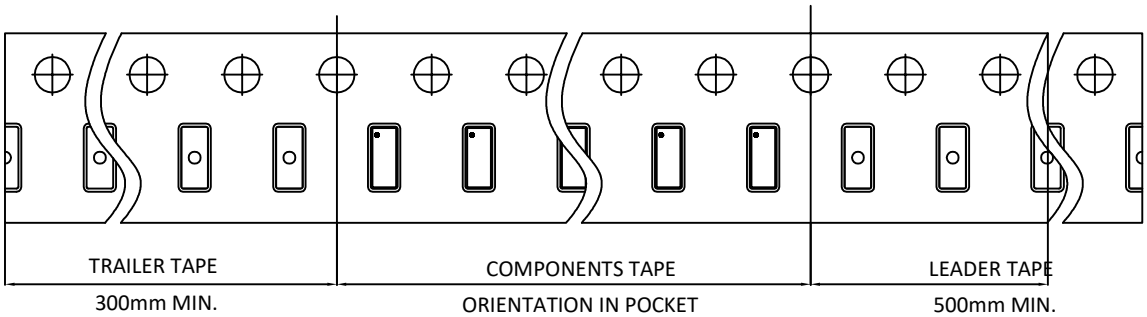
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	S	K	G	R
8	Ø178	Ø178.0 ±1.0	Ø60.0 ±1.0	11.80 ±0.5	9.0 ±0.5	Ø13.0 +0.5 -0.2	2.40 ±0.10	10.25 ±0.2	Ø9.8	---

DFN2.5x1.0_10L_EP2_S/DFN2.5x1.0A_10L_EP2_S Tape

Leader / Trailer & Orientation

Unit Per Reel: 3000pcs



All Dimensions Comply with EAI-481